EN0-001 Q&As

ARM Accredited engineer

Pass ARM EN0-001 Exam with 100% Guarantee

Free Download Real Questions & Answers **PDF** and **VCE** file from:

https://www.certbus.com/en0-001.html

100% Passing Guarantee
100% Money Back Assurance

Following Questions and Answers are all new published by ARM Official Exam Center

QUESTION 1

Many ARM cores provide two instruction sets, ARM and Thumb. Which THREE of the following statements apply to the Thumb instruction set implemented for the ARMv7-A architecture? (Choose three)

A. Thumb is a hybrid 16/32-bit instruction set

B. No Thumb instructions can be conditionally executed

C. Thumb code is always slower than the equivalent ARM code

D. Some routines take more instructions in Thumb code than in the equivalent ARM code

E. The Thumb instruction set can access the Advanced SIMD "NEON" instructions

F. Thumb code is always more power-efficient than equivalent ARM code

Correct Answer: ADE

QUESTION 2

When using the Performance Monitoring Unit to count runtime events the counter registers are limited to 32-bits. How can more than 2A32 events be counted without significantly impacting the software performance?

A. Register an interrupt which is triggered when the counter overflows

B. Count the events using a 64-bit VFP register

C. Allow one event type to use concatenated counter registers

D. Poll the event counter, resetting it when the counter is close to overflowing

Correct Answer: A

QUESTION 3

The Performance Monitoring Unit (PMU) of a Cortex-A9 processor permits direct measurement of which one of the following?

A. Cache Size

B. Clock Speed

C. Program size

D. Numbers of instructions executed

Correct Answer: D

QUESTION 4

A software profiling tool records the address held in the Program Counter (PC) every 1 ms. The software function that resides at each recorded address can be determined by the profiling tool. The percentage of time spent in each function is calculated from the percentage of recorded addresses where each function is resident.

Which one of the following statements is FALSE?

A. The tool shows an estimate of the percentage of time spent in each function

B. The tool identifies all functions executed by the application

C. The function with the highest percentage is a good candidate for optimization

D. The results will be more accurate on a processor running at 250 MHz. than one running at 2 GHz

Correct Answer: B

QUESTION 5

An ARMv7 implementation might include the VFPv4-D32 floating point extension. What does the \\'32\\' indicate?

A. The width of the datapath in bits

B. The number of double precision floating point registers implemented

C. The number of bits of data that can be loaded or stored at once

D. The number of integer operations that can be performed simultaneously

Correct Answer: B

QUESTION 6

The following C function is compiled with hard floating point linkage.

float function(int a, float b, int c, float d);

Which register is used to pass argument c?

A. R0

B. R1

C. R2

D. R3

Correct Answer: B

QUESTION 7

Optimizing for space will:

A. Produce an image which is decompressed at run-time.

B. Cause the compiler to unroll loops where possible.

C. Result in more functions being inlined by the compiler.

D. Produce smaller code, even if this results in slower execution.

Correct Answer: D

QUESTION 8

Capturing processor execution trace is characterized as being:

A. Influenced by breakpoints.

B. Intrusive on normal processor operation.

C. Inaccurate regarding code execution history.

D. Not intrusive on normal processor operation.

Correct Answer: D

QUESTION 9

In an operating system environment, most applications are executed in which processor mode?

A. Supervisor

B. IRQ

C. System

D. User

Correct Answer: D

QUESTION 10

What is an "Entry point" in an application?

A. A place where execution can start

B. The location of the main () function

C. The lowest address contained in a program image

D. A location where the linker can store additional information

Correct Answer: A

QUESTION 11

If the performance of an application remains unchanged when the core clock speed of a Cortex-A9 processor is reduced, what can you deduce about the system?

A. The Clocks Per Instruction (CPI) of the processor has increased

B. The processor is NOT the limiting factor on performance

C. Instruction cache utilization has improved

D. The core has stopped carrying out speculative data memory accesses

Correct Answer: B

QUESTION 12

When the processor is executing in Thumb state, which of the following statements is correct about the values stored in R15?

A. Bits[31:16] are duplicated with bits[15:0]

B. The PC value is stored in bits[31:1] and bit[0] is treated as zero

C. The PC value is stored in bits[31:16] and bits[15:0] are undefined

D. The PC value is stored in bits[15:0] and bits[31:16] are undefined

Correct Answer: B

QUESTION 13

Which of the following operations would count as intrusive to normal processor operation?

A. Tracing using Embedded Trace Macrocell (ETM)

B. Halt mode debugging

C. Monitor mode debugging

D. Using the Performance Monitor Unit

Correct Answer: B

QUESTION 14

In Thumb state an ARMv7-A processor can execute:

A. Only 16-bit Thumb instructions.

B. Only 32-bit Thumb instructions.

C. 16-bit and 32-bit Thumb instructions.

D. 32-bit Thumb and certain ARM instructions.

Correct Answer: C

QUESTION 15

An advantage of removable flash memory over built-in flash memory is that:

A. Storage can be easily replaced, for example to increase capacity.

B. It is quicker to access, providing far greater bandwidth for read operations.

C. It has a longer life, indicated by being rated for a higher number of write cycles.

D. It takes up less physical space in a device, and does not require any space on the printed circuit board.

Correct Answer: A